Date: 30.12.2019

Indira Gandhi Delhi Technical University for Women

(Established by Govt. of Delhi vide Act 09 of 2012)

Kashmere Gate, Delhi - 110006

ICT based One Week STC on "Design Challenges in Low Power VLSI Design"

Department of Electronics & Communication Engineering. (ECE), I G DT UW , Kashmere G ate organized one week JCT based Short Term Programme on "Design Challenges in Low Power VLSI Design" in collaboration with NITTTR Chandigarh during I 6th - 20th December , 20 19 . The venue of the Programme was DSP Lab , Room No. I 09, ECE Department. Course Content covered in one week JCT based Short Term ProgrammeChallenges in low Power Des ign , IC Fabr ic atio n, Evolutionary Approach to VLSI CAD, Concepts of Low Power Design, Concepts of Low Power Design, VHDL Programming, Nano Scale Semi-Conductor Dev ices , Low Power Memory Des ig n, Cogenda T-CAD, Cogenda T-CAD, Cogenda T-CAD, Advances in materials for VLSI Application, VLSI Devices for Low Power App lica tions .T he program was exceptionally beneficial for the faculty members of EC E\departmen t. The FOP was attended by nearly 48 part ici pants including fac u lties , lab assistants.30 M tec h students and 28 research scholars also attended the FOP .

Co-ordinator

Dr Richa Yadav
Assistant professor
Department of ECE, IGDTUW